

REMARKS

Applicants thank Examiner for their detailed review of the application. Applicants have made amendment to the specification within paragraph 0017 to correct a typographical error. Examiner objected to the drawings under 37 CFR 1.84(p)(5) because there was no mention in the description of reference characters 520. Applicants have submitted replacement drawing sheets removing reference characters 515 and 520.

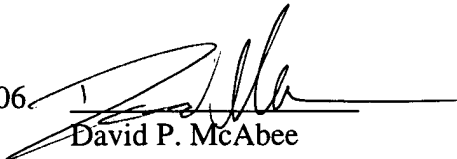
Examiner also rejects claims 1-24 as being indefinite under 35 U.S.C. § 112, second paragraph. Applicants have amended claim 1 to include etching a via opening and a trench opening and forming a conductive material in the via opening and the trench opening. Applicants particularly point out and claims forming a zeolite-CDO film for damascene processing steps, such as etching and forming, as referenced above. Claim 19 also includes similar limitations, referencing forming a zeolite-CDO composite interlayer dielectric. Therefore, applicants respectfully submit that claims 1 and 19, as well as their dependent claims, sufficiently point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner also rejects claims 1-7, 9-21, and 23-24 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2005/0236714, herein referred to as Leu et al. Applicants note that U.S. Patent Application Publication No. 2005/0236714, which was filed on June 28, 2005, is a divisional application of Application of Ser. No.: 10/302,073 filed Nov. 21, 2002, which was issued as U.S. patent number 6,943,121 on September 13, 2005. Leu et al., which is cited under 35 U.S.C. 102(e), and applicants' application are commonly assigned to Intel Corporation. Therefore, with respect to the 102(e) rejection to claims 1-7, 9-21, and 23-24, applicant is filing a terminal disclaimer in reference to U.S. 6,943,121 filed November 21, 2002.

Please charge any shortages and credit any overcharges to our Deposit Account No.
02-2666.

Respectfully submitted,
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